In the Claims:

1. (Currently Amended) A method of forming a semiconductor structure, the method comprising:

providing a substrate;

forming a polysilicon layer on the substrate;

treating the polysilicon layer with ammonia;

oxidizing exposed portions of the polysilicon layer; and

removing the exposed portions of the polysilicon layer, wherein the oxidized portions of the polysilicon layer act as a mask.

2. (Original) The method of claim 1, wherein the substrate has one or more shallow trench isolations formed therein and an oxide layer formed on the substrate.

3. (Original) The method of claim 1, wherein the polysilicon layer is formed by low-pressure chemical vapor deposition.

4. (Original) The method of claim 1, wherein the step of treating the polysilicon layer is about 500 Å to about 3000 Å in thickness.

5. (Original) The method of claim 1, wherein the step of oxidizing is performed by wet thermal oxidation.

6. (Original) The method of claim 1, wherein the semiconductor structure is a split-gate transistor.

7. (Original) The method of claim 1, wherein the step of oxidizing includes masking the polysilicon layer to define one or more structures.

8. (Original) The method of claim 7, wherein the step of masking is performed by forming and patterning a layer of silicon nitride.

9. (Original) The method of claim 8, wherein the layer of silicon nitride is about 400 Å to about 4000 Å in thickness.

10-16. Cancelled.

17. (Original) An split-gate transistor comprising:

a control gate;

a floating gate, the floating gate being formed of polysilicon that has been treated with ammonia;

a poly-oxide layer formed on the floating gate; and

an inter-poly oxide formed on the floating gate and the poly-oxide layer, being positioned between the control gate and the floating gate.

18. (Original) The apparatus of claim 16 wherein the split-gate transistor is a portion of a memory cell.

19. (Original) The apparatus of claim 16 wherein the floating gate is about 500 Å to about 3000 Å in thickness.

20. (Original) The apparatus of claim 16 wherein the poly-oxide layer is about 500 Å to about 3000 Å in thickness.

21. (Original) The apparatus of claim 16 wherein the poly-oxide is formed of polysilicon that has been oxidized.

22. (Original) The apparatus of claim 16 wherein the floating gate has been treated with ammonia by a thermal anneal process or a rapid thermal anneal process.